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PLAYBK-ROUTINES TO DRIVE A DIGITAL-TO-ANALOG CONVERTER

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DAVID W. TAYLOR NAVAL SHIP RESEARCH AND DEVELOPMENT CENTER

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PLAYBK-ROUTINES TO DRIVE A DIGITAL-TO-ANALOG CONVERTER

by

James R. Carlberg

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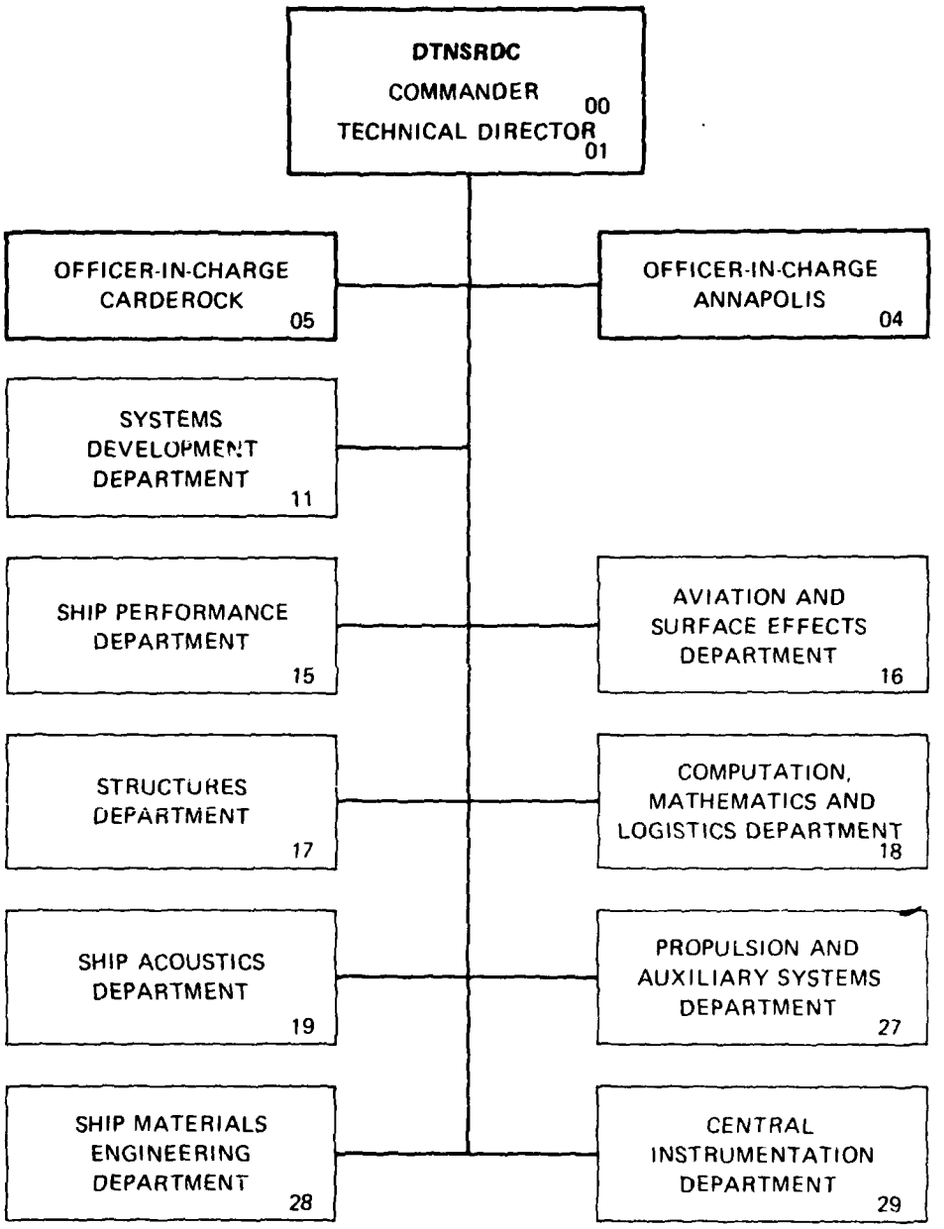

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Two software drivers have been written to control a digital-to-analog (D/A) converter on a PDP-11/45 minicomputer. One driver is a stand-alone program which outputs user specified data to the D/A converter at a user specified rate and scale factor. The second driver is a FORTRAN callable controller where the calling program specifies the data buffer, rate, and scale factor. This report is a user's document describing the procedure for using the controllers.

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ABSTRACT

Two software drivers have been written to control a digital-to-analog (D/A) converter on a PDP-11/45 minicomputer. One driver is a stand-alone program which outputs user specified data to the D/A converter at a user specified rate and scale factor. The second driver is a FORTRAN callable controller where the calling program specifies the data buffer, rate, and scale factor. This report is a user's document describing the procedure for using the controllers.

INTRODUCTION

Code 1824 under the direction of Dr. Sidney Berkowitz has been developing computer programs to analyze and classify acoustic transients. These programs run on a PDP-11/45 using GT-11 interactive graphics. Many times we have felt that hearing specified signal segments would help in developing transient classifiers. To this end, two programs have been written to control a digital-to-analog (D/A) converter option in the PDP's Laboratory Peripheral System.[1] The output of the D/A converter can be low-pass filtered and input to an audio amplifier with a loudspeaker for playback.

The two D/A control programs drive the D/A using specified data at a specified rate with a specified scale factor. One driver is a stand-alone program that takes data from a user specified PDP file and outputs the data to the D/A converter at a user specified rate and scale factor. The other driver is a FORTRAN callable version where the calling program, via call parameters, specified the data buffer, rate, and scale factor. This note provides brief descriptions of the D/A hardware, and the procedure for using the programs.

---

[1] "LPS11 Laboratory Peripheral User's Guide", Digital Equipment Corporation, 1974.

HARDWARE DESCRIPTION

The digital-to-analog (D/A) converter is included as part of the Laboratory Peripheral System interfaced to the PDP-11/45. This note deals with the LPSVC display controller and the LPSKW programmable real-time clock. Complete descriptions of these are given in "LPS11 Laboratory Peripheral System" manual supplied by Digital Equipment Corporation. The LPSVC and the LPSKW are described in chapters 5 and 3 respectively.

The LPSVC Display Control is an option for the Lab Peripheral System that permits the control of a display. The LPSVC provides 4096_{10} discrete points in both the X and Y directions. The heart of the LPSVC are X and Y D/A converters. Output operations are accomplished by loading the X or Y register with the 12-bit value to be converted to an analog voltage. The output range for each converter is from -5 volts to +5 volts. The input to each converter must be coded in offset binary. Table 1 shows the inputs required to generate -5, 0, and +5 volts outputs.

Input (OCAL)	Output (Volts)
0000	-5
4000	0
7777	+5

Table 1. D/A Conversion Code

The LPSVC outputs are available through a back panel connector labeled DISPLAY. The X analog output is available at pin 24 with the analog ground at pin 25. The Y analog output is available at pin 21 and its analog ground is at pin 22. The LPSVC Unibus addresses are shown in Tab e 2. Currently, the D/A driver programs use only the X D/A converter.

LAB PERIPHERAL SYSTEM DEVICE	UNIBUS ADDRESS (OCTAL)
LPSKW Status Register (clock)	770404
LPSKW Buffer (clock)	770406
LPSVC Status Register (D/A)	770416
LPSVC X Register (D/A)	770420
LPSVC Y Register (D/A)	770422

Table 2. Device Unibus Addresses

The LPSKW Real-Time Clock offers the Lab Peripheral System methods for accurately measuring time intervals. The drivers use the clock in the repeated interval mode to control the time interval between samples sent to the D/A converter. The base frequency used for the clock counter is dependent upon the user specified D/A output rate. The clock provides interrupt, as each time interval ends. When an interrupt occurs a sample is sent to the D/A converter. The LPSKW Unibus addresses are shown in Table 2. The interrupt trap region starts at address 344 (OCTAL).

STAND-ALONE PROGRAM

The file named PLAYBK.SAV is a stand-alone D/A driver program. This program reads data from a user specified file and outputs each point at a user specified rate to the LPSVC X register D/A converter. The rate is specified in points per second (Hertz). The user must also supply a scale factor which specifies which 12 consecutive bits of each 16-bit data point are to be converted. The program prints out a header describing the codes for selecting the conversion bits where bit 15 is the most significant bit and bit 0 is the least significant bit. A typical user-program sequence is shown in figure 1 where the program responses are underlined. When the program has finished converting the last data point, the "FINISH RUN--" message is printed and the program recycles to the beginning, asking the user for a new file name. To convert another file, the user must specify the file name, the bit code, and the output rate. If the output rate is the same as the previous rate, the user can enter a carriage return. The program can be exited by entering a control C.

```
.RUN DPO:PLAYBK
PDP LAB.  PERIPHERAL SYSTEM PLAYBACK PROGRAM
        *D/A XREG
        BIT CODES FOR SELECTING 12 CONVERSION BITS
                0-LOW ORDER 12 BITS
                1-      BITS 12 TO 1
                2-      BITS 13 TO 2
                3-      BITS 14 TO 3
                4-HIGH ORDER 12 BITS
ENTER FILE NAME:  *DPO:SINE
ENTER BIT CODE:   0
ENTER D/A RATE IN HZ (<CR> FOR PREVIOUS RATE):  10000
FINISH RUN--
ENTER FILE NAME:  *
```

Figure 1. PLAYBK.SAV Program-User Dialog Example.

Three types of errors can occur while data are being converted. If a D/A hardware error occurs, the "D/A HARDWARE ERROR--" is printed, conversions are stopped, and the program recycles back to the beginning, asking the user for a file name. If a read error occurs when data are obtained from the file, the "FILE READ ERROR--" message is printed, conversions are stopped, and the program recycles back to the beginning, asking the user for a file name. A

read overlap error occurs when data are read from disk more slowly then the data are outputed to the D/A converter. The D/A converter is temporarily stopped until the last read is completed and a "WAIT--" message is printed. The D/A is restarted at the interrupted point. Tests indicate the program can run at rates up to 19000 hertz without a read overlap occuring.

The other error types occur when an error is detected in a user entered specification. These errors include a file specification error, a bit code error, and a rate specification error. The specified file must be an existing file on the requested device. The bit code for specifying the scale factor must be between zero and four. Two types of rate specification errors can occur. First the specified rate must be less than 32768 so it can fit in one 16-bit word. The slowest rate is one hertz. The other rate specification error occurs when the user requests the previous rate and there had been no previous rate.

FORTRAN CALLABLE HANDLER

The file named DAHDLR.OBJ is the object file containing the FORTRAN callable entry points to drive the D/A converter. This file is linked with program object files to create the run time module. The only restriction in using the handler is the code must not be overlayed from the time the call to set up the D/A is made until the completion call is made to terminate conversions.

The object file contains three FORTRAN callable entry points. The first entry point is used to set up the D/A. The calling parameters for this entry point specify the output rate in samples per second, the scale factor in terms of left shift bits, the number of points per buffer, and an error code. The error code allows the calling program to monitor the state of the driver. The form of the call is

```
CALL SETDA (IRATE, NWORDS, NSHIFT, ICODE)
```

where

IRATE is an INTEGER*2 value specifying the D/A output rate in points/second

NWORDS is an INTEGER*2 value specifying the number of words per data buffer (The data buffer is specified in the PLAYBK call).

NSHIFT is an INTEGER*2 value specifying the output scale factor.

```
=0  Low order 12 bits output
=1        bits 12 to 1 output
=2        bits 13 to 2 output
=3        bits 14 to 3 output
=4  High order 12 bits output
```

ICODE is an INTERGER*2 value returned indicating the drivers state.

```
=1  Conversions from buffer in progress
=0  Buffer conversions complete. D/A will continue to output
    the last value of the last buffer.
=-1 D/A hardware error.
```

The call to SETDA turns on the D/A converter. The output will be zero volts until the data buffer is specified.

The second entry point specifies the data buffer from which values are sent to the D/A converter. The output rate and the number of words per buffer must have been specified with the SETDA call. The form of the call is

```
PLYBK (IBUFR)
```

where

IBUFR is an INTEGER*2 value of the first point in the data buffer to be converted.

The call to PLAYBK initiates the D/A conversions from the specified buffer and returns control to the calling program. PLAYBK can be recalled at any time with a new buffer specification. PLAYBK will wait until the first buffer conversions are finished, then initiate the D/A conversions from the second buffer. Control will be returned to the calling program once the conversions from the second buffer are initiated. If the conversions from the first buffer are completed prior to the specification of the second buffer, the driver will continuously output the last value of the first buffer until the second buffer is specified. ICODE is set to one during the time the D/A converter is outputting data from a buffer; otherwise ICODE is zero, unless a D/A hardware error occured then ICODE=-1. Note, the calling program should not modify data in a buffer until the conversions from that buffer are completed.

The final entry point terminates the D/A conversions. The interrupts are disabled. The form of this call is

```
CALL DACOMP
```

A word of warning must be restated before the D/A handler is used. The calling programs must not cause the D/A driver to be overlayed from the time a call to SETDA is made until a call to DACOMP is made. If the D/A drivers are overlayed during D/A operations, the results will be catastrophic.

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